D. Remarks

Objections to Claims.

Claims 5 and 6 have been amended to address the claim objections.

The claims have been amended as suggested by the Examiner.

Rejection of Claims 1-6 Under 35 U.S.C. §103, based on *Christensen et al.* (USP 5,889,306) in view of *Wyborn et al.* (USP 5,587,339).

The semiconductor device of claim 1 includes a low resistance embedded wiring layer and a plurality of element regions. The low resistance embedded wiring layer is formed on and extending over a semiconductor substrate. The plurality of element regions are formed over the embedded wiring layer separated from one another and having at least one circuit element formed therein. Each element region is in contact with the embedded wiring layer.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

Applicant believes a prima facie case cannot exist, as the combination of references does not show or suggest all the limitations of claim 1.

As noted in the rejection, *Christensen et al.* does not teach or suggest a low resistance embedded wiring layer.[2] Therefore, *Christensen et al.* cannot teach or suggest a plurality of element regions formed over the embedded wiring layer or that each element region being in contact with the embedded wiring layer as recited in claim 1. *Christensen et al.* shows transistors, but such transistors are never shown or suggested to be over any wiring layer or in contact with such an embedded wiring layer.

However, the other reference relied upon by the rejection, *Wyborn et al.*, does not show such limitations either. *Wyborn et al.* shows a multi-level metallization process including a selective tungsten deposition process for forming tungsten contacts.[3] There is no teaching or suggestion that circuit elements are formed over this multi-level metallization. Therefore,

---

[1] MPEP §2143.

[2] See page 3, 2nd to last paragraph of Office Action dated 12/29/04.

[3] See Fig. 5 of *Wyborn et al.* showing wiring layer 2 and wiring layer 20 having a contact 18 formed therebetween by a selective tungsten deposition process.

Wyborn et al. does not teach or suggest the low resistance embedded wiring layer in which a plurality of element regions (having at least one circuit element formed therein) are formed over the low resistance embedded wiring layer as required in claim 1.

It is noted that the proposed combination of references cannot arrive at Applicant's claim 1 invention. The rejection proposes the following:

> It would have been obvious... to form a low resistance... interconnect layer extending over a silicon substrate, as taught by Wyborn to incorporate into Christensen's structure to arrive the claimed limitation in order to provide low resistivity contacts (col. 5, line 16). (Office Action, dated 12/29/05, Page 4, Lines 7-10).

The above combination does not indicate how element regions would be formed over such a wiring layer. That is, the rejection cannot have established a prima facie case that the references teach placing element regions over an interconnect layer.

Because the references do not teach or suggest all the claim limitations of claim 1, this ground of rejection is traversed.

Claims 5 and 6 have been amended not in response to the cited art, but to address informalities.

The present claims 1-14 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

March 23, 2005

Darryl G. Walker
Attorney
Reg. No. 43,232

Darryl G. Walker
WALKER & SAKO, LLP
300 South First Street
Suite 235
San Jose, CA 95113
Tel. 1-408-289-5314